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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Heer	Docket No.:	2002 P 10624 US
Serial No.:	10/724,011	Art Unit:	2129
Filed:	November 26, 2003	Examiner:	Peter D. Coughlan
For:	Arrangement of Configurable Logic Blocks		

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

This Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed June 19, 2006. A Notice of Appeal was filed by facsimile on September 19, 2006. A petition for a two-month extension of time is being submitted concurrently herewith.

REAL PARTY OF INTEREST (37 C.F.R. 41.37(c)(1)(i))

The present application is assigned to Infineon Technologies AG.

RELATED APPEALS AND INTERFERENCES (37 C.F.R. 41.37(c)(1)(ii))

Appellant is not aware of any related appeals or interferences.

STATUS OF CLAIMS (37 C.F.R. 41.37(c)(1)(iii))

Claims 1-14 stand finally rejected. No claims have been allowed. Therefore, claims 1-14 are the subject of this appeal. The claims on appeal are reproduced in the Claims Appendix. These claims do not include any amendments requested in the concurrently filed amendment.

STATUS OF AMENDMENTS (37 C.F.R. 41.37(c)(1)(iv))

An amendment correcting non-substantive errors is being filed concurrently herewith. The issues raised in this brief are not affected by the entry of the amendment. A Pre-Appeal Brief Request for Review was filed on September 19, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. 41.37(c)(1)(v))

The preferred embodiment of the invention provides a solution to the problem of minimizing the use of area for configurable logic blocks (CLB) and is achieved by adapting its corresponding components to the functional task of the CLB. Par. [0015], line 1, page 6. Thus, in the solution of the problem according to embodiments of the invention, a CLB contains a first and/or second look up table with content addressability, which implements the switching function of at least one conditional branch. Par. [0015], line 3, page 6. This conditional branch generates an "if then else" branch, which realizes a comparison of CLB input data with comparison data previously stored in the CLB. Par. [0015], line 6, page 6.

In a first aspect, as defined by claim 1, the invention provides an arrangement of configurable logic blocks (CLB) in customer-specific circuits. Referring to the figure, an input data node 1 carries input data. Par. [0024], line 1, page 8. A CLB control logic circuit 8 has a first input (coupled to input data node 1), a second input (coupled to control input node 10), a third input (coupled to comparator 6 or 16 of look-up table 2 or 12), a fourth input (coupled to multiplexer 3 or

13) and an output. At least one look up table 2 and/or 12, implements a switching function of at least one conditional branch, with content addressability. Par. [0015], line 5, page 6.

The at least one look-up table 2 and/or 12 generates an "if then else" branch that realizes a comparison of the input data with comparison data previously stored in the at least one look-up table 2 and/or 12. Par. [0015], line 6, page 6. A result output of the at least one look up table 2 and/or 12 is provided to the third input of the CLB control logic 8. Par. [0026], line 3, page 9. For the look-up table 2, this third input can be seen as the second line from the bottom on the left-hand side of the CLB control logic circuit 8, which line came from the comparator 6 of look-up table 2.

An input data bus 7 is coupled between the input data node 1 and a bus input of the at least one look up table 2 and/or 12. Par. [0024], line 1, page 8. The bus input of the look-up table 2 is shown in the figure as the line going into look-up table 2 between register 4 and comparator 6. The first input of the CLB control logic circuit 8 is coupled to the input data node 1 via the input data bus 7. Par. [0024], line 5, page 8.

At least one multiplexer 3 and/or 13 has a control input coupled to the input data node 1 and also to the first input of the CLB control logic circuit 8 via at least part of the bit width of the input data bus 7. Par [0024], line 3, page 8. An output of the at least one multiplexer 3 and/or 13 is coupled to the fourth input of the CLB control logic circuit 8. Par. [0024], line 5, page 8. For the multiplexer 3, this third input can be seen as the third line from the bottom on the left-hand side of the CLB control logic circuit 8, which line came from the multiplexer 3.

A control input node 10 is coupled via a control bus 17 to the second input of the CLB control logic circuit 8. Par. [0024], line 6, page 9. This second input is shown as connecting to the bottom of the block 8. At least one register data bus 5 is coupled between a register data bus output

of the at least one look up table 2 and/or 12 and a bus input of the at least one multiplexer 3. Par. [0015], line 6, page 6.

In the embodiment of claim 2, the at least one look up table 2 and/or 12 is realized with the conditional branch implemented in it by such a switching function. Par. [0015], line 6, page 6. The at least one look up table 2 and/or 12 includes a register 4 which stores the comparison data and a comparator 6 coupled to the input data node and the register. Par. [0023], line 2, page 8. The comparator 6 is operable to compare the input data with the comparison data. Par. [0026], line 1, page 9.

In the embodiment of claim 3, the bus input of the at least one look up table 2 and/or 12 is coupled to a first bus input of the comparator 6 and/or 16 and wherein a bus output of the register 4 and/or 14 is coupled to a second bus input of the comparator 6 and/or 16 and also to the register data bus output of the at least one look up table 2 and/or 12. An output of the comparator 6 and/or 16 is coupled to the result output of the at least one look up table 2 and/or 12. Par [0026], line 1, page 9.

In the embodiment of claim 4 the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology. Par. [0028], line 2, page 10.

In the embodiment of claim 5, the output of the CLB control logic circuit 8 serves as an output of the CLB. Par [0026], line 6, page 9.

Claim 6 is the second independent claim. This claim recites a logic circuit that includes, a register 4, and a comparator 6 with a first input coupled to the register 4 and with a second input coupled to an input node 1. Par [0025], line 1, page 9. A multiplexer 8 with an input is coupled to the register 4. Par. [0025], line 3, page 9. A control block includes inputs coupled to the multiplexer 3, the comparator 6, the input node 1 and a control input node 10. Par. [0026], line 4,

page 9. The logic circuit realizes an "if then else" branch based upon information carried at the input node 1 and information stored in the register 4. Par. [0028], line 6, page 10.

In the embodiment of claim 7, the logic circuit comprises a configurable logic block. Par. [0028], line 2, page 10.

In the embodiment of claim 8, the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology. Par. [0028], line 2, page 10.

In the embodiment of claim 9, the logic circuit also includes, a second register 14, and a second comparator 16 with a first input coupled to the second register 14 and with a second input coupled to the input node 1. Par. [0025], line 3, page 9. A second multiplexer 13 includes an input coupled to the second register 14. Par. [0025], line 3, page 9. The control block 8 is coupled to the second comparator 6 and the second multiplexer 13. Par. [0026], line 4, page 9.

In the embodiment of claim 10, the output of the control block 8 serves as an output of the logic circuit. Par. [0026], line 6, page 9.

Claim 11 is the final independent claim. This claim recites a logic circuit that includes, means for performing a switching function of at least one conditional branch is implemented with content addressability. Par. [0015], line 5, page 6. The means for performing a switching function generates an "if then else" branch that realizes a comparison of input data with previously stored comparison data. *Id.* This embodiment also includes means for selecting at least a portion of the comparison data is coupled to the means for performing a switch function. Par. [0025], line 3, page 9. A CLB control logic circuit 8 has a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting. Par. [0026], line 1, page 9.

Claim 11 includes means-plus-function language in accordance with 35 U.S.C. § 112, sixth paragraph. The means for performing a switching function can be implemented by lookup table 2. Par. [0015], line 5, page 6. The means for selecting can be implemented by multiplexer 3. Par. [0025], line 3, page 9.

In the embodiment of claim 12, the means for performing a switching function comprise, means for storing the comparison data (e.g., register 4) and means for comparing the comparison data and the input data (e.g., comparator 6). Par. [0025], line 1, page 9.

In the embodiment of claim 13, the means for performing a switching function comprises a register 4 that stores the comparison data and a comparator 6 coupled to the register and to an input data node 1 that carries the input data. Par. [0025], line 1, page 9.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. 41.37(c)(1)(vi))

(1) Claims 1-10 stand rejected under 35 U.S.C. § 101 for non- statutory subject matter.

(2) Claims 1, 2, 4, 5, and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tseng (U.S. Publication No. 2002/0152060) in view of Mano ("Logic and Computer Design Fundamentals), further in view of Barstow (U.S. Patent No. 4,827,404), further in view of Hellstrand (U.S. Publication No. 2002/0019969) and further in view of Miller (U.S. Patent No. 6,181,164).

(3) Claim 3 stands rejected under U.S.C. § 103(a) as being unpatentable over the combination of Tseng, Mano, Barstow, Hellstrand and Miller and further in view of Udagawa (U.S. Patent No. 6,388,767).

(4) Claims 6, 7, 8, 9, 10 stand rejected under U.S.C. § 103(a) as being unpatentable over the combination of Tseng, Mano, Barstow, Hellstrand and Miller and further in view of Nataraj (U.S. Publication No. 2002/0161969).

(5) Claims 11, 12, 13 stand rejected under U.S.C. § 103(a) as being unpatentable over the combination of Tseng, Mano, Barstow, Hellstrand and Miller and further in view of Nomura (U.S. Patent No 6,317,363).

ARGUMENT (37 C.F.R. 41.37(c)(1)(vii))

It is respectfully submitted that claims 1-14 recite patentable subject matter under the provisions of 35 U.S.C. §§ 101 and 103. The rejection under Section 101 will be discussed first followed by a discussion of the each claim in view of the prior art. Any claim not explicitly argued stands or falls with the claim from which it depends. Finally, in an abundance of caution, Appellant will discuss the drawings, which have been discussed in the final rejection without having been rejected.

1. Claims 1-10 recite statutory subject matter

Claims 1-10 and 14 have been finally rejected under 35 U.S.C. § 101 "for non-statutory subject matter". Final rejection, page 3. Appellant respectfully submits that the product claims in the present application are directed to statutory subject matter.

Section 101 provides that a patent may be obtained for "any new and useful process, machine, manufacture or composition of matter." Claim 1 is directed to an arrangement that includes an input data node, a CLB control logic circuit, a look-up table, an input data bus, a multiplexer, a control input node and a register data bus. These are all tangible, concrete things.

Similarly, claim 6 is directed to a logic circuit that includes a register, a comparator, a multiplexer and a control block. Once again, these are tangible things.

The final rejection states that the "invention is ineligible because it has not been limited to a substantial practical application." Final rejection, page 3 (emphasis in original). According to the final rejection, "the focus is not on whether the steps taken to achieve a particular result are useful, tangible and concrete, but rather that the final result achieved by the claimed invention is 'useful, tangible and concrete.'" *Id.* (emphasis in original).

Appellant notes that the cited test is directed to whether "steps" recite a particular result that is useful, tangible and concrete. The present claimed invention has no steps. Rather, it is directed to a device. The elements of the claims, some of which are listed above, are clearly tangible and concrete. As a result, the final result is tangible and concrete.

Further, the claimed invention is useful. For example, embodiments of the invention provide a solution to the problem of minimizing the use of area for configurable array blocks. Par. [0015]. As another example, one configuration shows its advantage in that for the implementation of more than one conditional branch in an LUT, an additional savings of hardware resources is achieved by reducing the required CLBs. Par. [0021].

The final rejection states that an arrangement of logic blocks or a logic circuit has no defined practical application. Final rejection, page 3. Appellant respectfully disagrees. As stated in the Background, Field Programmable Logic Devices (FPLD) have been an integral component for digital circuit implementation. Par. [0002]. As discussed above, the present patent application provides a number of examples of advantages provided by the present invention.

The claims clearly recite subject matter that has a practical application. Contrary to the characterization of the final rejection, claim 1 does not recite merely an arrangement of

configurable logic blocks. Rather claim 1 recites a very specific arrangement, i.e., one that includes an input data node, a CLB control logic circuit, a look-up table, an input data bus, a multiplexer, a control input node and a register data bus arranged in a specific manner. Similarly, claim 6 recites a register, a comparator, a multiplexer and a control block. Both of these claims have practical applications. The patent law makes no requirement that these practical applications be delineated in the claim.

In fact, claims 4 and 8 specifically recite that the claimed apparatus is realized in Field Programmable Gate Array (FPGA) technology. This very particular technology is certainly a practical application that merits patentable subject matter. In fact, the patent office itself has created classification 716/16, which explicitly lists FPGA along with other similar technologies. Certainly, a technology that has no defined practical application would not warrant specific mention in the classification manual.

Accordingly, Appellant respectfully submits that all of the claims recite statutory subject matter.

2. Claim 1 is not obvious over the combination of five prior art references

Independent claim 1 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Tseng, Mano, Barstow, Hellestrand and Miller. Appellant respectfully submits that the combination of five unrelated references cannot be used to teach or suggest the claimed invention.

Of course, there is no limit to the number of references that can be used in a valid Section 103 rejection. In this case, five references have been relied upon to show the six of the seven

elements of claim 1[1]. Of significant importance, none of these references provide any teaching or suggestion that they can be combined. In particular, the Office Action relies upon:

1. Tseng, which describes an interchip communication system;
2. Mano, a textbook entitled *Logic and Computer Design Fundamentals*;
3. Barstow, which describes software to implement an if-then function;
4. Hellestand, which shows a virtual processor; and
5. Miller, which describes a programmable gate array.

A review of the rejection makes clear that the combination of references is inappropriate. An element by element analysis will now be performed.

Input data node – The Examiner and Appellant agree that Tseng teaches an input data node.

CLB control logic circuit – The Examiner and Appellant agree that Tseng does not teach a CLB control logic circuit. To find such a circuit, the Examiner looks to the register selection circuit shown in Figure 7-5 of Mano, stating that the "CLB control logic can be anything."[2] The asserted suggestion to combine is based on the conclusion that:

> It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify teachings of Tseng by having a control unit that uses current input to dictate the operations of the CLB as taught by Mano to have a CLB control circuit having a first input, a second input, a third input, a fourth input and an output.

Final rejection, page 5. The Examiner points to nothing in the references that provides any suggestion that the references can be combined. The suggestion to combine must appear in the references themselves. MPEP § 2143.01.

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[1] As discussed below, the rejection fails to make any showing of one of the elements.

[2] The final rejection states that the four inputs are K1, K2. Of course, K1 and K2 are only two inputs.

At least one look-up table – The Examiner and Appellant agree that neither Tseng nor Mano teaches at least one look-up table. The rejection instead looks to Barstow, which teaches a method and system for computer programming, and summarily concludes that the combination would be obvious "[f]or the purpose of having the ability to identify a if-then-else statement." Final rejection, page 6. No citation to any reference is provided to show any motivation to combine.

"The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." MPEP §2143.01 III, citing In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). In this case, it is not even clear that the references can be combined. For example, Mano is directed to a circuit that includes an OR gate, a multiplexer and a register load; Barstow to computer programs implemented, for example, in "an object-oriented language." There is nothing in the record even alleging that one of ordinary skill in the art would know how to modify the combinational logic of Mano to implement the software functions of Barstow.

An input data bus – The Examiner contends that Tseng "teaches an input data bus coupled between the input data node and a bus input of the at least one look-up table." Final rejection, page 7. Appellant respectfully disagrees given that Tseng "do[es] not teach at least one look-up table ...." Final rejection, page 6. The reference certainly cannot teach a bus coupled to an element that the Examiner admits is not taught by the reference.

At least one multiplexer – The Examiner admits that "Tseng, Mano and Barstow do not teach at least one multiplexer ... ." Instead, the Examiner looks to Hellestrand, which teaches hardware and software co-simulation including simulating the cache of a target processor. Once again, there is no teaching or motivation taught by the references. The Examiner's rationale for the

combination is "[f]or the purpose of operating with current inputted data results in improved results." Final rejection, page 8.

Even if one accepts that the goal of each of the references is to achieve "improved results," the references provide no teaching that their combination would provide any improvements. The present application is the only document that teaches the claimed combination and it is black letter law that the motivation to combine cannot be found within the present invention. The Examiner's unsupported and conclusory statements are unsupported and improper.

A control input node - The final rejection provides no indication that any of the references teach or suggest a control input node. Rather, the final rejection refers to the claim rejection under 35 U.S.C. § 112. Final rejection, page 8. A review of the prosecution history shows that there has been only one section 112 rejection, which applied to claim 6. The final rejection unequivocally states that "Examiner withdraws the 35 U.S.C. § 112, first paragraph rejection." *Id.*, page 22. Since the Examiner has failed to show one of the claimed elements, the rejection must be withdrawn. This basis alone is sufficient to overturn the rejection.

At least one register data bus – The Examiner admits that "Tseng, Mano, Barstow and Hellestrand do not teach at least one register data bus ..." but looks to Miller, which teaches a linear feedback shift register in a programmable gate array. Final rejection, page 8. As before, there is no suggestion to combine the references.

In summary, a Section 103 rejection cannot be sustained by simply finding each of the elements in different, unrelated references. "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references

themselves or in the knowledge generally available to one of ordinary skill in the art." MPEP §2143.01. In this case, no teaching, suggestion or motivation exists.

3. Claim 2 is not obvious over the combination of five prior art references

Claim 2 specifically recites that the at least one look up table is realized with the conditional branch implemented in it by such a switching function and that the at least one look up table comprises a register which stores the comparison data; and a comparator coupled to the input data node and the register, the comparator operable to compare the input data with the comparison data. The references of record do not teach or suggest the limitations of claim 2.

To show the elements of this claim, the Examiner goes through the Mano textbook, which is entitled "Logic and Computer Design Fundamentals," and finds a register on page 351 in the chapter entitled "Resistor Transfers and Data Paths" and an AND gate (allegedly a comparator) on page 29 in the chapter entitled "Combination Logic Circuits." Appellant freely admits that registers and comparators were known prior to the present invention. That is not the issue. The issue is whether it would have been obvious to implement the claimed look-up table using a register and a comparator as recited in claim 2.

In the rejection, the Examiner asserts that Barstow teaches a look-up table. There is no assertion that any other reference teaches or suggests this element. In Barstow, the invention is implemented in a computer system, e.g., as shown by the target process of Figure 1. The Examiner has provided no explanation as to how the teachings of Barstow can be modified to implement a look-up table using a register and comparator as required by claim 2. Instead, the Examiner summarily concludes that it would have been obvious to modify Tseng. This conclusion, however, is irrelevant. The Examiner admits that Tseng does not teach or suggest a look-up table. It is

therefore impossible to modify the non-existent look-up table to be implemented as required by claim 2.

4. Claim 3 is not obvious over the combination of six prior art references

Claim 3 specifically recites that "the bus input of the at least one look up table is coupled to a first bus input of the comparator and wherein a bus output of the register (4), (14) is coupled to a second bus input of the comparator and also to the register data bus output of the at least one look up table, and wherein an output of the comparator is coupled to the result output of the at least one look up table."

Claim 3 limits how the comparator and register of the look-up table are coupled with the remainder of the circuit. According to the rejection of claim 2, this comparator and register are taught by Mano. Rather than look to Mano, or any of the four other references, the Examiner looks to Udagawa, which relates to an image processing apparatus. The references, however, provide no teaching or suggestion that the photocopier circuitry of Udagawa can be combined with the teachings of the other references.

5. Claim 4 is not obvious over the combination of five prior art references

Claim 4 specifically recites that "the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology." The Examiner states that "Tseng does not teach the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology."[3]

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[3] Appellant notes the Tseng teaches an inter-chip communication system that transfers signals across FPGA chip boundaries. Par. [0019]. Appellant agrees that Tseng does not teach that the claimed configurable logic blocks can be realized in FPGA technology.

Instead, the Examiner looks to a different chapter of the Mano textbook for the proposition that FPGA technology was known prior to the present invention. Once again, Appellant does not dispute that FPGA technology was known. What was not known was the implementation of the specifically claimed arrangement realized in FPGA technology. As a result, claim 4 is allowable.

6. Claim 6 is not obvious over the combination of six prior art references

Independent claim 6 specifically recites a logic circuit that includes a register, a comparator, a multiplexer, and a control block, in a specific configuration, "wherein the logic circuit realizes an 'if then else' branch based upon information carried at the input node and information stored in the register." Appellant respectfully submits that this claim is allowable.

The rejection states "Tseng does not teach a register, a comparator ...; a multiplexer." The rejection continues by looking to different chapters of the Mano textbook, which show a register, a comparator and a multiplexer. The rejection then somehow reaches the conclusion that "[i]t would have been obvious ... to modify the teachings of Tseng by connecting the components of a register, comparator, a multiplexer as taught by Mano to have [the elements as claimed]." Final rejection, page 13. The reason this would be obvious is "[f]or the purpose of comparing input values to aid in the execution of the 'if-then-else' logic." *Id.*

Appellant is at a loss on how to respond. The Examiner admits that the primary reference teaches none of the claimed elements. Further, the alleged reason motivation to combine, to aid in the execution of the 'if-then-else' logic, is also not taught in any the references. The rejection makes no assertion to the contrary.

Appellant admits that, prior to the present invention, registers were known. Further, comparators were known. So were multiplexers and control blocks. "If then else" functions were

also known. Appellant submits, however, that the claimed combination of these known elements was not known. Nothing close to a showing to the contrary has been made.

None of the references teaches or suggest any combination of the claimed elements. Further, none of the references provides any teaching or suggestion as to how or why the claimed elements should be combined. As a result, claim 6 is allowable.

7. Claim 7 is not obvious over the combination of six prior art references

Claim 7 specifically recites that "the logic circuit comprises a configurable logic block." This claim has been rejected because "Mano teaches the logic circuit comprises a configurable logic block." Final rejection, page 14. Appellant respectfully disagrees.

The cited circuit on page 351 of Mano illustrates a block diagram and detailed logic for the use of multiplexers to select between two registers. There is no teaching that this circuit is a configurable logic block. Since none of the references teaches the claimed limitation, the combination of references cannot teach the claimed limitation and, therefore, claim 7 is allowable.

8. Claim 8 is not obvious over the combination of six prior art references

Claim 8 specifically recites that "the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology." The Examiner states that "Tseng does not teach the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology." As with claim 4, the Examiner looks to the "Memory and Programmable Logic Devices" chapter of the Mano textbook for the proposition that FPGA technology was known prior to the present invention. Once again, Appellant does not dispute that FPGA technology was known. What was not known was the implementation of the specifically claimed arrangement realized in FPGA technology. As a result, claim 8 is allowable.

9. Claim 9 is not obvious over the combination of six prior art references

Claim 9 specifically further requires "a second register; a second comparator ...; a second multiplexer ... ; and wherein the control block is coupled to the second comparator and the second multiplexer." In other words, claim 9, which depends from claim 6, requires both a multiplexer (as recited in claim 6) and a second multiplexer (as recited in claim 9).

To show these elements, the Examiner points to page 351 of the Mano textbook, which shows a circuit that includes only a single multiplexer. Even ignoring the fact that there is no teaching to combine the elements in the claimed manner, the combination of references clearly fails to teach all of the elements, e.g., at least two multiplexers. As a result, claim 9 is allowable.

10. Claim 11 is not obvious over the combination of six prior art references

Independent claim 11 specifically recites

> means for performing a switching function of at least one conditional branch is implemented with content addressability, wherein the means for performing a switching function generates an "if then else" branch that realizes a comparison of input data with previously stored comparison data;
>
> means, coupled to the means for performing a switch function, for selecting at least a portion of the comparison data; and
>
> a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting.

This claim was rejected over Tseng, Mano, Barstow, Hellstrand, Miller and Nomura. The Examiner admits that Tseng, Mano, Hellstrand and Miller do not teach any of the claimed elements. The Examiner concludes, however, it would be obvious to modify the combined teachings of Tseng and Mano based upon the teachings of Barstow. As discussed above, Tseng teaches inter-chip communications, Mano is a basic textbook on logic circuits and Barstow is a software patent.

Appellant respectfully submits that, first, it would not be obvious to combine the teachings of Tseng and Mano. Even if it were, it would not be obvious to modify the circuits of Tseng and Mano with the software of Barstow.

Further, claim 11 recites a CLB control logic circuit. The Examiner admits that Tseng, Mano, Barstow, Hellstrand and Miller teach no such circuit. Rather, the Examiner looks to Nomura, which teaches a non-volatile memory device. In particular, the Examiner looks to a switching circuit that selects which memory cell in an array will be programmed. This reference is completely unrelated to any of the other cited references much less the claimed invention.

It is respectfully submitted that claim 11 is allowable.

11. Claim 12 is not obvious over the combination of six prior art references

Claim 12 specifically recites that "the means for performing a switching function comprises: means for storing the comparison data; and means for comparing the comparison data and the input data." Appellant respectfully submits that claim 12 is allowable over the references of record.

As noted above, the Examiner admits that Mano does not teach the means for performing a switching function. According to the Examiner, this element is taught by Barstow. However, the rejection of claim 12, which claim further defines the means for switching, never mentions Barstow. Clearly, any appropriate rejection would provide a rationale as to how the means for switching in Barstow could be modified to meet the limitations of claim 12. No such rationale has been provided. It is therefore respectfully submitted that claim 12 is allowable.

12. Claim 13 is not obvious over the combination of six prior art references

Claim 13 specifically recites that "the means for performing a switching function comprises: a register that stores the comparison data; and a comparator coupled to the register and to an input

data node that carries the input data." Appellant respectfully submits that claim 13 is allowable over the references of record.

As noted above, the Examiner admits that Mano does not teach the means for performing a switching function. According to the Examiner, this element is taught by Barstow. However, the rejection of claim 12, which claim further defines the means for switching, never mentions Barstow. Clearly, any appropriate rejection would provide a rationale as to how the means for switching in Barstow could be modified to meet the limitations of claim 13. No such rationale has been provided. It is therefore respectfully submitted that claim 13 is allowable.

13. The drawings meet the requirements of the patent law

Page 2 of the final rejection states

> 4. In the non-final office action the Examiner stated there were 6 inputs for the CLB control logic and the claims state there are only 4 inputs. Per the application the CLB control logic is item #8 in figure #1. The CLB control logic has 6 inputs, bus 17 from input node 10, bus 7 from input node 1, the output of register 3, the output of register 6, the output of register 16, and the output of register 13, totaling 6 inputs into the CLB control logic 8.

Appellant and Examiner agree on the count of the number of inputs into CLB control logic 8 of the lone figure in the application. Where Appellant and Examiner appear to disagree is in the statement that "the claims state there are only 4 inputs." Nowhere do the claims state that there are only four inputs. The claims state what they state.

For example, claim 1 recites "a CLB control logic circuit having a first input, a second input, a third input, a fourth input and an output." The CLB control logic circuit 8 clearly has a first input (coupled to input data node 1 via the input bus 7), a second input (coupled to control input node 10 via control bus 17), a third input (coupled to the output of look-up table 2) and a fourth input (coupled to the output of multiplexer 3).

Rule 83 requires that the drawing must show every feature of the invention specified in the claim. The drawing clearly does. As a result, the drawings meet the requirements of the patent law. Appellant notes that nothing requires that the claim specify every feature shown in the drawings.

In the Response to Arguments section of the final rejection, the Examiner states:

> The logic circuit that performs the 'if-then-else' function only needs the components diagrammed in figure 1. If the invention described by the application performs some additional function other than the 'if-then-else' function then this is not declared in the applicants claims. First Office Action stands.

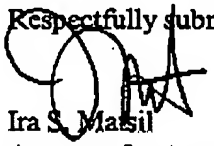
The invention is defined by the claims. In other words, the invention is what is recited in the claims - nothing more, nothing less. There is no requirement that everything that is described in an application must be specified in all the claims.

CONCLUSION

For the foregoing reasons, Appellant respectfully submits that the final rejection of claims 1-14 under 35 U.S.C. § 103 and claims 1-10 under 35 U.S.C. § 101 is improper and respectfully requests that the Board of Patent Appeals and Interference so find and reverse these rejections.

To the extent necessary, Appellant petitions for an Extension of Time under 37 C.F.R. § 1.136. Please charge any fees, or credit any overpayments, in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 50-1065.

Respectfully submitted,



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CLAIMS APPENDIX

1. (Previously Presented) An arrangement of configurable logic blocks (CLB) in customer-specific circuits, the arrangement comprising:

an input data node for carrying input data;

a CLB control logic circuit having a first input, a second input, a third input, a fourth input and an output;

at least one look-up table in which a switching function of at least one conditional branch is implemented with content addressability, wherein the at least one look-up table generates an "if then else" branch that realizes a comparison of the input data with comparison data previously stored in the at least one look-up table, and wherein a result output of the at least one look-up table is provided to the third input of the CLB control logic;

an input data bus coupled between the input data node and a bus input of the at least one look-up table, wherein the first input of the CLB control logic circuit is coupled to the input data node via the input data bus;

at least one multiplexer having a control input coupled to the input data node and also to the first input of the CLB control logic circuit via at least part of the bit width of the input data bus, an output of the at least one multiplexer being coupled to the fourth input of the CLB control logic;

a control input node coupled via a control bus to the second input of the CLB control logic; and

at least one register data bus coupled between a register data bus output of the at least one look-up table and a bus input of the at least one multiplexer.

2. (Original) The arrangement of claim 1, wherein the at least one look-up table (2), (12) is realized with the conditional branch implemented in it by such a switching function, and wherein the at least one look-up table (2), (12) comprises:

a register which stores the comparison data; and

a comparator coupled to the input data node and the register, the comparator operable to compare the input data with the comparison data.

3, (Original) The arrangement of claim 2 wherein the bus input of the at least one look-up table is coupled to a first bus input of the comparator and wherein a bus output of the register (4), (14) is coupled to a second bus input of the comparator and also to the register data bus output of the at least one look-up table, and wherein an output of the comparator is coupled to the result output of the at least one look-up table.

4. (Original) The arrangement of claim 1 wherein the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology.

5. (Original) The arrangement of claim 1 wherein the output of the CLB control logic serving as an output of the CLB.

6. (Previously Presented) A logic circuit comprising:

a register;

a comparator with a first input coupled to the register and with a second input coupled to an input node;

a multiplexer with an input coupled to the register; and

a control block with inputs coupled to the multiplexer, the comparator, the input node and a control input node, wherein the logic circuit realizes an "if then else" branch based upon information carried at the input node and information stored in the register.

7. (Original) The circuit of claim 6 wherein the logic circuit comprises a configurable logic block.

8. (Original) The circuit of claim 7 wherein the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology.

9. (Original) The circuit of claim 6 and further comprising:

a second register;

a second comparator with a first input coupled to the second register and with a second input coupled to the input node;

a second multiplexer with an input coupled to the second register; and

wherein the control block is coupled to the second comparator and the second multiplexer.

10. (Original) The circuit of claim 6 wherein the output of the CLB control logic serving as an output of the logic circuit.

11. (Original) A logic circuit comprising:

means for performing a switching function of at least one conditional branch is implemented with content addressability, wherein the means for performing a switching function generates an "if then else" branch that realizes a comparison of input data with previously stored

comparison data;

means, coupled to the means for performing a switch function, for selecting at least a portion of the comparison data; and

a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting.

12. (Original) The circuit of claim 11 wherein the means for performing a switching function comprises:

means for storing the comparison data; and

means for comparing the comparison data and the input data.

13. (Original) The circuit of claim 11 wherein the means for performing a switching function comprises:

a register that stores the comparison data; and

a comparator coupled to the register and to an input data node that carries the input data.

14. (Original) The circuit of claim 1 wherein the logic circuit is realized in Field Programmable Gate Array (FPGA) technology.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None